REMARKS

Applicant gratefully acknowledges the Examiner's statement that claims 22-27 contain allowable subject matter. No claims have been amended. Claims 1-45 remain pending in this application.

Claims 1-21, 28-34 and 36-45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Roth (U.S. Patent No. 6,771,525). The rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a content addressable memory (CAM) comprising "match combining circuitry that responds to the match signals and to a signal indicating a search width that is a multiple of the location width, the match combining circuitry providing combined match signals, each combined match signal indicating a combination of a group of match signals, the combination depending on the indicated search width." Claim 1 further recites "priority encoder circuitry that responds to the CAM array, providing priority signals indicating at most one group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion." Applicant respectfully submits that Roth fails to disclose the claimed invention.

Roth generally refers to a CAM that selectively combines match line latch outputs from two adjacent CAM memory arrays and provides the combined outputs to a multiple match resolver/priority encoder in response to a variable word width control signal. Roth does not disclose or suggest a CAM having "match combining circuitry that responds . . . to a signal indicating a search width that is a multiple of the location width." Roth also fails to disclose providing "combined match signals, . . . the combination depending on the indicated search width." The claimed invention logically combines groups of match signals and thus, obtains combined match signals

that depend on a search width indicated by bit length. This is simply not shown in Roth.

Nor does Roth disclose or suggest "priority encoder circuitry that responds to the CAM array, providing priority signals indicating at most one group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion." Roth simply refers to its priority encoder and multiple match resolver choosing the hit having the highest priority address and providing that highest priority address as the output. Nothing in Roth discloses or suggests "priority encoder circuitry" as in the claimed invention. For at least the reasons set forth above, Roth does not anticipate the claim 1 invention.

Independent claims 5, 9, 13, 20, 28, 36, 38, 40, 41 and 43 recite limitations similar to the "priority encoder circuitry" discussed above. Independent claims 17, 31, 34, 39 and 44 recite limitations similar to the "match combining circuitry" described above. Independent claims 7, 29, 34 and 37 recite limitations similar to both the "priority encoder circuitry" and "match combining circuitry" described above. For at least the same reasons as set forth above, all independent claims should be allowable. Claims 2-4 depend from claim 1 and are allowable along with claim 1. Claim 6 depends from claim 5 and are allowable along with claim 5. Claim 8 depends from claim 7 and are allowable along with claim 7. Claims 10-12 depend from claim 9 and are allowable along with claim 9. Claims 14-16 depend from claim 13 and are allowable along with claim 13. Claims 18 and 19 depend from claim 17 and are allowable along with claim 17. Claim 21 depends from claim 20 and is allowable along with claim 20.

Accordingly, Applicant respectfully requests that the rejection be withdrawn and claims 1-21, 28-34 and 36-45 be allowed.

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Roth in view Ichiriu (U.S. Patent No. 6,901,000). The rejection is respectfully traversed.

Claim 35 recites similar limitations as recited above relating to claim 1. For at least the reasons set forth above, Roth fails to teach or suggest a CAM having "match combining circuitry that responds . . . to a signal indicating a search width that is a multiple of the location width," and provides "combined match signals, . . . the combination depending on the indicated search width." Nor does Roth teach or suggest "priority encoder circuitry that responds to the CAM array, providing priority signals indicating at most one group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion."

The Office Action seeks to overcome the shortcomings of Roth by combining it with Ichiriu. The Office Action cites Ichiriu as teaching lower and upper address encoding circuitry. (Office Action at 4). However, Applicant respectfully submits that Ichiriu does not cure the shortcomings of Roth. That is, Ichiriu does not teach or suggest "match combining circuitry that responds . . . to a signal indicating a search width that is a multiple of the location width," and provides "combined match signals, . . . the combination depending on the indicated search width," or "priority encoder circuitry that responds to the CAM array, providing priority signals indicating at most one group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion."

Therefore, the cited combination fails to teach or suggest all limitations of the claimed invention, and thus does not render obvious the claimed invention.

Accordingly, Applicant respectfully requests that the rejection be withdrawn and claim 35 allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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